Journal of Basic and Applied Engineering Research
p-ISSN: 2350-0077; e-ISSN: 2350-0255; Volume 3, Issue 12; October-December, 2016, pp. 1106-1110

http://www.krishisanskriti.org/Publication.html

Design of Low Power High Speed 1- Bit Hybrid Full Adder

Shikha Singh[1] and Ashutosh Kumar Singh[2]

[1]M. Tech (VLSI Design) NIET Greater Noida, India
[2](ECE) NIET Greater Noida, India
E-mail: [1]shikhaec07@gmail.com, [2]singhashu1986@gmail.com

Abstract—*Full adders are the fundamental unit in any digital system. Adders are used for arithmetic calculations so if we improve performance parameters for full adder the speed of arithmetic logic unit can be increased. But main problem with an adder circuit is carry generation and propagation that induce delay in circuit. If we induce carry propagation time, delay can be minimized.*
In this proposed circuit a hybrid 1-bit full adder is designed using Complementary Pass Transistor Logic and Transmission Gate Logic using 180nm CMOS technology and then it is extended to 32-bit also. The circuit is implemented using Tanner EDA tool of 13.1 version. Performance parameters such as delay, power consumption and Power Delay Product were compared with existing hybrid 1-bit full adder using complementary-CMOS and TGL design. The result shows improvement of 11.16% in delay,34.63% in power consumption and 24.14% in PDP.

Keywords*: 32-bit Ripple Carry Adder, Tanner EDA, PDP, Transmission gate logic, Complementary pass transistor logic.*

1. INTRODUCTION

The days had been passed when room size computers were used for fastest computation but now a day's power consumption and compatibility is of major concern as everybody need handheld or portable devices with fast speed computation so there was a need of compatible device with more functions led to evolution of VLSI (very large scale integration).

Integrated circuit is a circuit where passive and active components can be implemented onto chip. Initially an IC could accommodate only few components but now a day we can fabricate billions of components on a single IC.

That lead to reduced size, high speed, lesser cost but power consumption is the area of concern. So there is a need of design that requires less area, good performance, low power consumption and dissipation.

1.2 Full Adder

Full adder is basically a small unit that performs the addition in any digital device work in filters and signals processing too. In full adder there are three modules are used with A, B, C_{in} are the Inputs and Sum, C_{out} as Outputs. Full adder always contain 3 modules module1 that is XOR gate that will generate the output as AB'+A'B and this output is been passed to module 2 and 3 simultaneously. Module 2 is provided with carry in addition from previous stage and this module will provide a sum as output. Module3 that is carry module will take the output from XOR in addition to that input carry and a input B that will provide the output as $AB + C_{in}AB + A'BC_{in}$.

Module1 is XOR Gate which take A,B as input and gives AB'+A'B as output that would be input to Module2,3 and C_{in} is another input to Module2,3 that will be sum and carry generator that provide the outputs as Sum and C_{out}

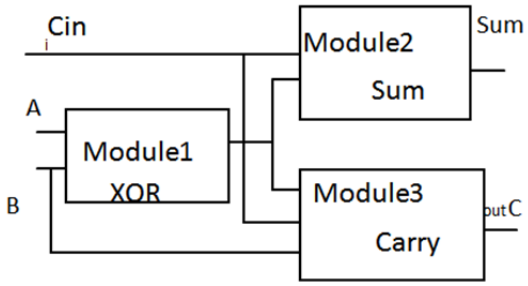

Fig. 1.1: Block Diagram of Full Adder

Where formula for the calculation of sum and carry would be:

$$Sum = AB' + B'A \quad (1)$$

$$Cout = AB + CinAB' + A'BCin \quad (2)$$

2. DESIGN APPROACH OF PROPOSED WORK

There are various designs available those have tradeoff between performance parameters one over other so we will use CPL and TGL to make hybrid design. CPL is complementary pass transistor logic and TGL is transmission gate logic. CPL have small carry propagation path so small delay, good voltage swing restoration but there are few problems with CPL techniques that it can be used only for high power application and gives high voltage degradation. This voltage degradation can be overcome by the TGL but still

some disadvantages like slow speed and high power consumption remain an area of concern so a new technique is applied called hybrid.

So we are proposing a modified circuit with better performance parameters that it reduced delay to 213.78ps and power to 4.54uW for 180nm technology at 1.8volt power supply. For 32 bit RCA circuit the delay is of 765ps and average power consumption is of 0.17uW.

In fig.-2.1 modified XNOR module is given which represent Module 1. In this design we are using 4 transistors only.

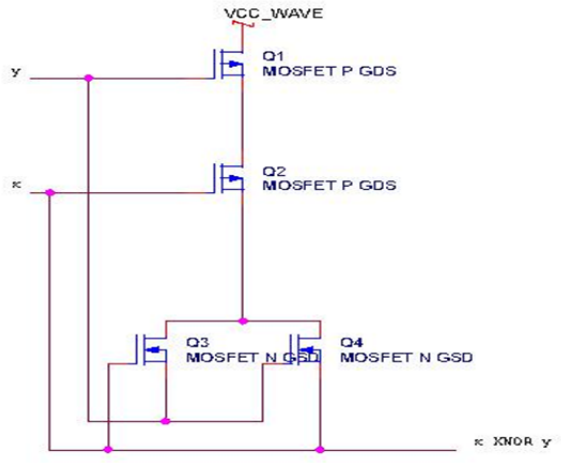

Fig. 2.1: Circuit diagram of modified XNOR module

In fig.- 2.2 1-bit hybrid full adder circuit is represented in which three inputs as A,B and cin is given and two outputs are taken as sum and cout.

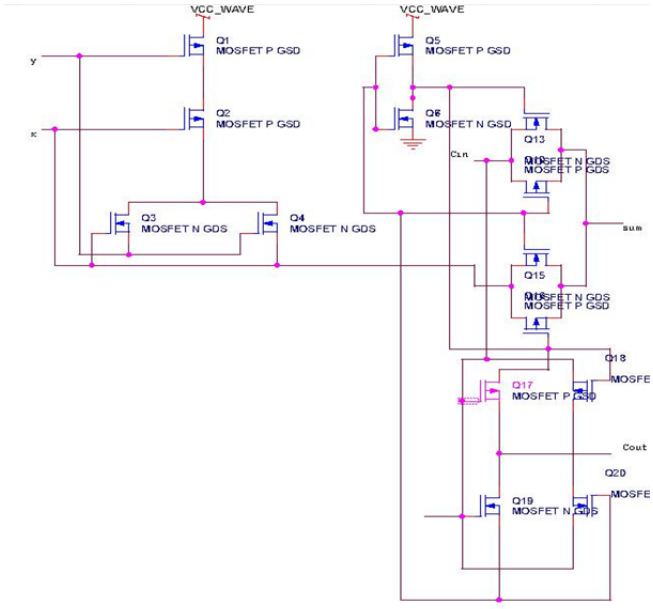

Fig. 2.2: Circuit diagram of the 1 bit hybrid full adder.

3. SIMULATION METHODOLOGIES

3.1 Performance Parameters:

Parameters of concern for backend are delay, PDP, power dissipation, area we need a design a circuit that is cost efficient and have better performance parameters then in base paper. Different logic styles tend to trade off with the performance of other. Performance parameters can be calculated by varying the width of each transistor one by one final width are seated and a table is formed to where every transistor is defined with the optimized width and length to get the most satisfactory results compared to existing design technologies. By reducing the size of transistor power also decrease but power and delay vary inversely.

3.2 Backend

We are using tanner EDA Tool so after the verification of a circuit on frontend we move on to backend with tanner EDA although there are many other costly tools available in market we will draw the schematic of modules for full adder that is provided in the base paper in S-edit using the software and initially we will divide the entire circuit into modules to elude further complications into results. Once we are done with S-edit the we will switch to W-edit automatically for the waveform generation to verify the circuit for each module we will compile the modules into a circuit and then than we will switch to LVS-edit automatically by giving the commands into S-edit here we can calculate the performance factors like delay, power etc here the real work begins when we have to change the width of transistors to get the better performance factors once we get the required results or approximate result then in L-edit we will get the layout of the circuit.

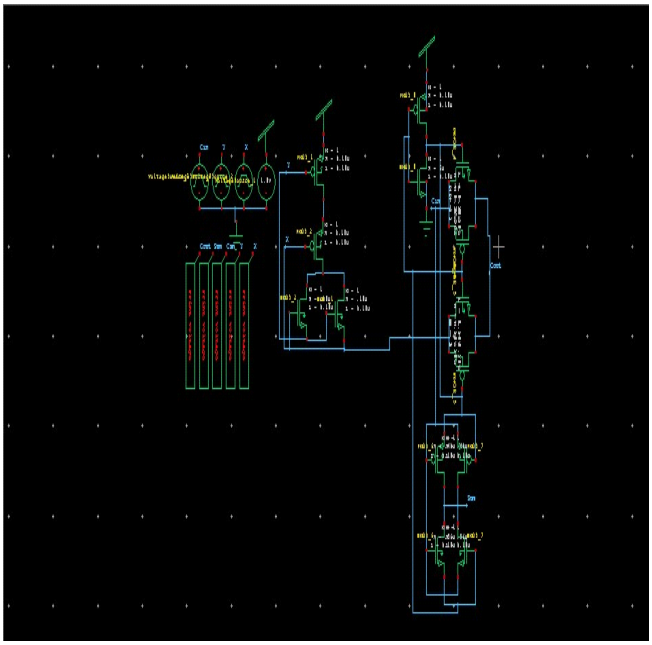

Fig. 3.1: Schematic for Modified Full Adder at 180nm Technology at 1.8 V

Once we done entire work on the 180nm technology then we will move on to 90nm technology then we will further reduce it to 45nm technology now we will check the parameters by making change in design technology or by making some amendments into it we can get better results and compact layout. Now the step is fabrication that is not done in India as it cost to high.

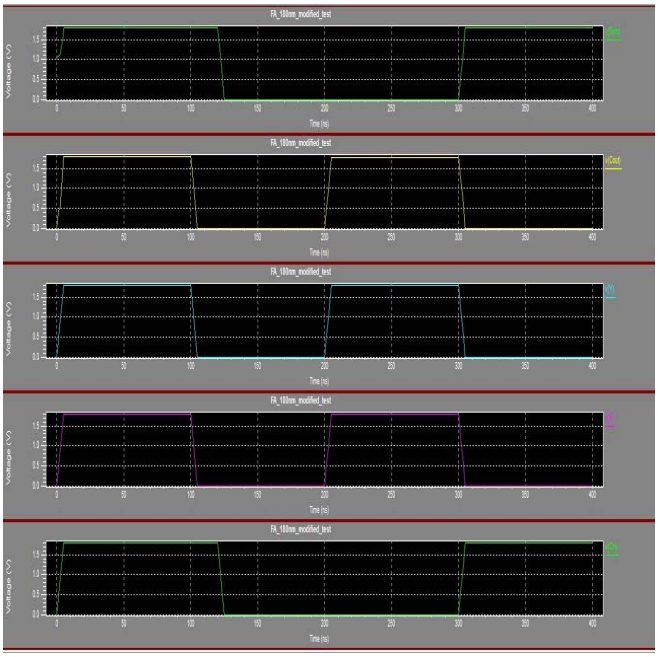

Fig. 3.2: Schematic for Modified Full Adder at 180nm Technology at 1.8 V

3.3 Proposed design for 32 bit RCA

A 32 bit Ripple Carry Adder consists of 32 full adders with the carry signal propagating from one full adder stage to the next from LSB to MSB. 32-bit full adder is implemented as an extension of proposed 1 bit full adder.

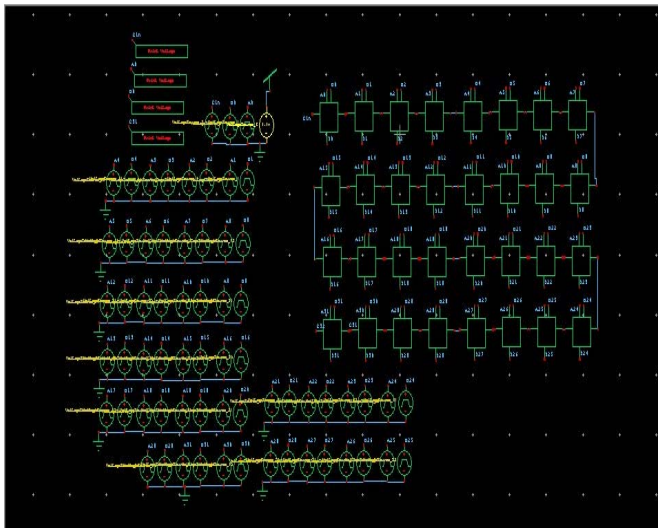

Fig. 4.1: Schematic for 32-bit RCA Full Adder on Tanner at 180nm Technology at 1.8 Volt Power Supply

The performance evaluation of this 32 bit adder was also carried out in 180 nm technology. The number of transistors used in this design is 448, delay is 765.33ps, average power is 0.17uW and PDP is 0.13fi. It is observed that the carry propagation delay increased almost linearly with 1 bit full adder.

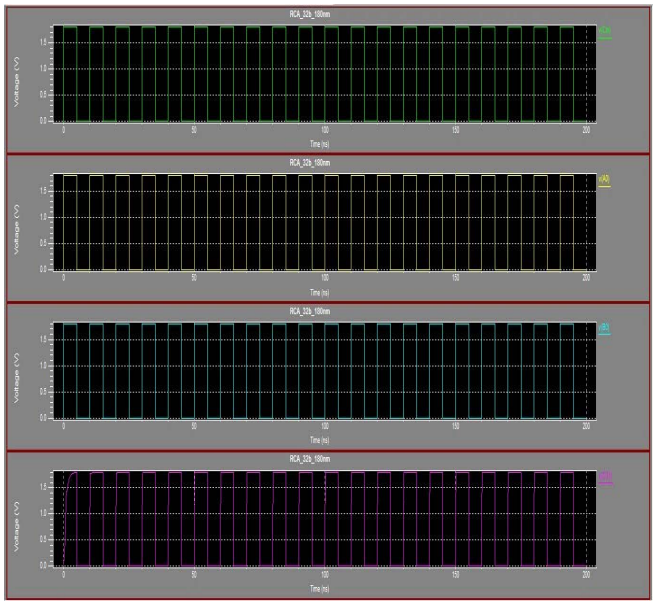

Fig. 4.2: Waveform for 32-bit RCA Full Adder module on Tanner

4. PERFORMANCE PARAMETERS ANALYSIS

Delay improvement of 11.16% for modified 1 bit full adder as compared to best design for hybrid full adder [3] and average power consumption reduction to 34.63%. As a ground always waste the power .A 32-bit carry propagation adder is implemented as an extension of the proposed 1-bit full adder. It is a non-carry look-ahead adder structure where the carry propagation takes place every time till the last adder block. Performance parameters can be calculated by varying the width of each transistor one by one final width are seated and a table is formed to where every transistor is defined with the optimized width and length to get the most satisfactory results compared to existing design technologies.

Table 5.1: Simulation result for full adder in 180 nm technologies at 1.8V.

Technologies	Delay (ps)	Average Power(μW)	PDP (fj)	Transistor	Reference
Hybrid full adder	241.25	4.6	0.931	16	[3]
32 bit RCA modified	765.33	0.17	0.13	448	proposed

Modified full adder 180nm	213.78	3.007	0.642	14	proposed

Graphical Comparison of delay for different adder design:-

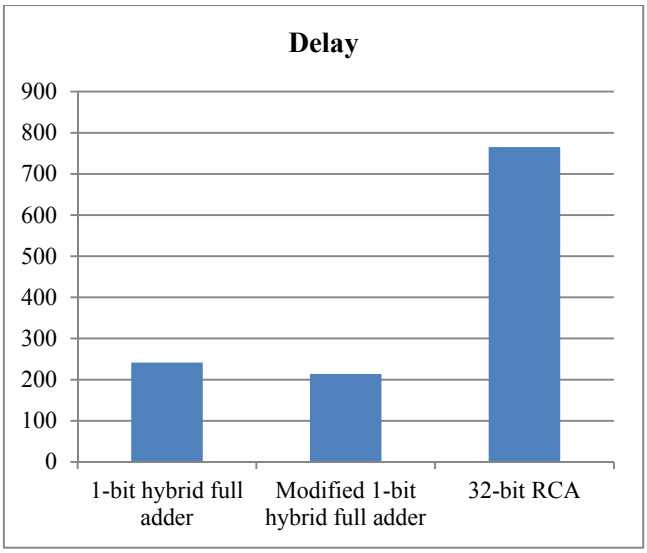

Fig. 5.1: Representing delay for full adder on different designs at 180nm Technology at 1.8 V power supply.

Graphical comparison of average power for Full Adder

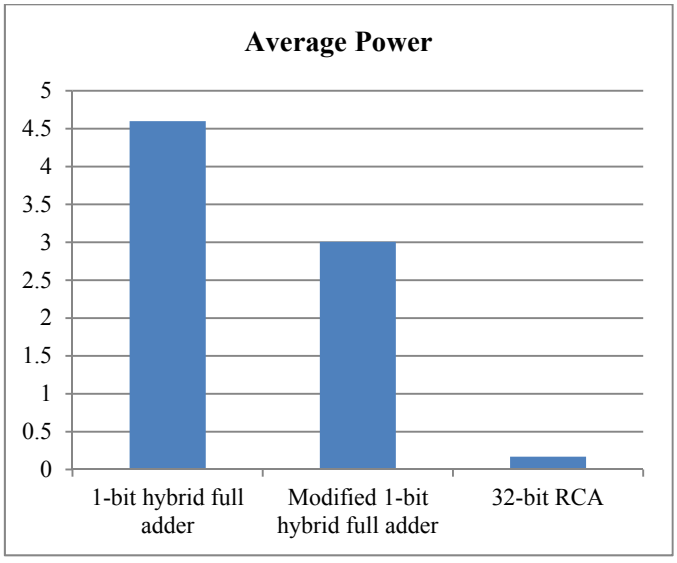

Fig. 5.2: Representing the comparison of average power of different designs at 180 nm technology.

Graphical comparison of PDP for Full Adder:-

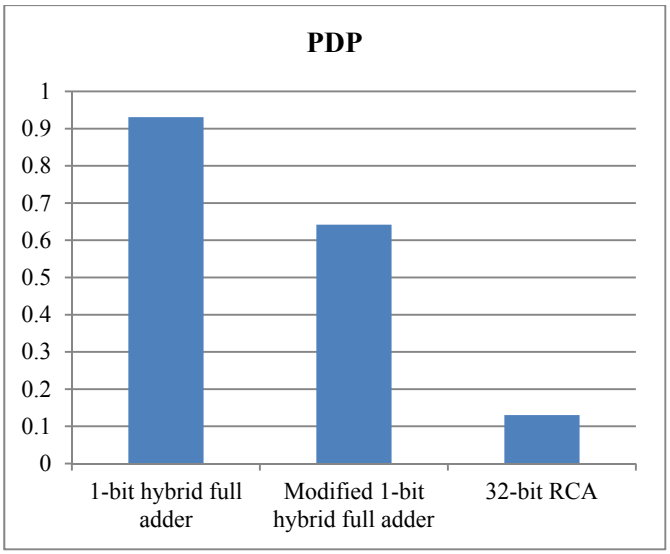

Fig. 5.3: Representing the comparison of PDP of different designs at 180 nm technology

5. CALCULATIONS

Average power can be calculated as the sum of both the static power and the dynamic power as well divided by 2.

$$P_{avg} = (P_s + P_d)/2 \quad \ldots(3)$$

PDP can be calculated as product of average power and delay.

$$PDP = P_{avg} \text{ X } D \quad \ldots (4)$$

P_{avg}: Average Power

$P_{s:}$ Static Power

P_d: Dynamic Power

PDP: Power Delay Product, D: Delay

6. CONCLUSION

In this thesis, we have studied the various designs of full adders at various design technologies. A high speed hybrid full adder is designed to overcome the problems of other designs for full adders and for fast execution of system we require an adder with less power dissipation. A low-power high speed modified hybrid 1-bit full adder has been proposed the design has been extended for 32-bit ripple carry adder also. The simulation was carried out using Tanner EDA tool with 180nm technology and has been compared with other standard design approaches like CMOS, CPL, 14T, TGA, and other hybrid designs. The simulation results established that the proposed modified adder offered improved PDP, delay, power consumption compared with the earlier reports. The efficient coupling of strong transmission gate driven by TPL complementary CMOS logic and removal of ground lead to fast switching speeds (213 ps at 1.8-V supply) in 180 nm

technology) excluding buffer. The proposed full adder offered 24.14% improvement with respect to the best reported design [25] in terms of PDP (180-nm technology at 1.8 V). The proposed full adder was further used to implement a 32-bit ripple carry propagation adder at 180nm technology at 1.8V. The numbers of transistors are also reduced. In proposed circuit we have modified a circuit out of best design circuit for hybrid full adder [25] that provides better performance in aspects of power, delay and PDP with lesser number of transistors at 180nm technology at 1.8V power supply. Even these have been further studied for 32 bit full adder that provides better results at 180 nm technology at 1.8 V power supply.

REFERENCES

[1] Majid Haghparast, Keivan Navi and Vahid Foroutan " A New Low Power Dynamic Full Adder Cell Based on Majority Function " World Applied Sciences Journal 4(1):133-141,2008

[2] Monico Linares-Aranda and Mariano Aguirre-Hernandez "CMOS Full-Adder for Energy Efficient Arithmetic Applications" IEEE transactions on very large scale integration systems (VLSI), Vol. 19, No.4, April 2011

[3] Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar and Anup Dandapat, " Performance Analysis of A Low Power High Speed Hybrid 1-bit Full Adder Circuit" IEEE transactions on Very Large Scale Integration Systems pp.1063-8210,2014 IEEE

[4] V. Vijay, J. Prathiba, S. Niranjan Reddy, P. Praveen Kumar "A Review of The 0.09um Standard Full Adders", International Journal of VLSI Design & Communication systems (VLSICS) Vol.3,No.3, June 2012

[5] Yi Wei, Ji Zhing Shen "Design of A Novel Low Power 8 Transistor 1 Bit Full Adder Cell", Univ-Sci C(Computer and Electron) 2011 12(7):604-607

[6] Manoj Kumar, Sandeep K. Arya and Sujata Pandey "Single Bit Full Adder Design using 8 Transistors with Novel 3 Transistors XNOR Gate" International Journal of VLSI Design & communication Systems Vol.2, No.4, December 2011

[7] J. M. Rabaey, A.Chandrakasan, and B.Nikolic, Digital integrated circuits: A design perspective, 2nd Edition India: Pearson Education, 2003.

[8] K. Navi, M. Maeen, V.Foroutan, S. Timarchi, and O. Kavehei, "A novel low power full-adder cell for low voltage" VLSI J. Integr., vol. 42, no. 4, pp. 457–467, Sep. 2009.

[9] D. Radha Krishnan, "Low-voltage low-power CMOS full adder," IEE Proc.Circuits Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.

[10] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus passtransistor logic," IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul.1997.

[11] C. H. Chang, J. M. Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686–695, Jun. 2005.

[12] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 1, pp. 20–29, Feb. 2002.

[13] M. Zhang, J. Gu, and C.-H. Chang, "A Novel Hybrid Pass Logic with Static CMOS Output Drive Full-Adder Cell," in Proc. Int. Symp. Circuits Syst., May 2003, pp. 317–320.

[14] S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energy efficient full adders for deep-sub micrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[15] H. T. Bui, Y. Wang, and Y. Jiang,"Design and analysis of low-power 10transistor full adders using novel XOR-XNOR gates," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, vol. 49, no. 1, pp. 25–30, Jan. 2002.

[16] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltage swing nodes," in Proc. IEEE Workshop Signal Process. Syst. (SiPS), Taipei, Taiwan, Oct 1999, pp. 713–722.